

CLAIMS:

1 1. A host-fabric adapter, comprising:

2 at least one Micro-Engine (ME) arranged to establish connections and support data

3 transfers, via a switched fabric, in response to work requests from a host system for data

4 transfers;

5 a context memory interface arranged to provide context information necessary for data

6 transfers; and

7 a doorbell manager arranged to update the context information needed for said Micro-
8 Engine (ME) to process said work requests for data transfers, via said switched fabric.

1 2. The host-fabric adapter as claimed in claim 1, wherein said context memory

2 interface comprises:

3 an address translator arranged to perform the address translation between a ME assigned
4 address and a memory physical address to access context information; and

5 a context memory having a bandwidth optimized, vertically sliced memory architecture
6 arranged to store context information needed for said Micro-Engine (ME) to process said work
7 requests for data transfers, via said switched fabric.

1 3. The host-fabric adapter as claimed in claim 2, wherein said context memory
2 contains a large quantities of context registers arranged to store context information needed for
3 said Micro-Engine (ME) to process said work requests for data transfers.

1 4. The host-fabric adapter as claimed in claim 3, wherein said Micro-Engine (ME),
2 said context memory interface, and said doorbell manager are configured in accordance with the
3 "*Virtual Interface (VI) Architecture Specification*", the "*Next Generation Input/Output (NGIO)*
4 *Specification*" and the "*InfiniBand™ Specification*".

1 5. The host-fabric adapter as claimed in claim 2, wherein said context memory
2 having a bandwidth optimized, vertically sliced memory architecture is partitioned vertically into
3 multiple memory slices based on a register width requirement, each of which supplies respective
4 bits of data of a predetermined register width to said Miro-Engine (ME), via a system bus of said
5 predetermined register width, and a number of registers of each of said multiple memory slices
6 corresponds to a designated number needed by network device requirements.

1 6. The host-fabric adapter as claimed in claim 2, wherein said Micro-Engine (ME),
2 said context memory interface, and said doorbell manager are implemented as part of an
3 Application Specific Integrated Circuit (ASIC).

1 7. The host-fabric adapter as claimed in claim 2, wherein said context memory
2 having a bandwidth optimized, vertically sliced memory architecture is partitioned vertically into
3 multiple memory slices based on a register width requirement, each of said memory slices
4 contains registers corresponding to a total number of registers of a designated size provided by
5 data network requirements, each of said memory slices has a register width selected to supply
6 respective bits of data to said Micro-Engine (ME), via a system bus of a predetermined register
7 width, and a register depth selected to correspond to the total number of registers of said
8 designated size, and all of said memory slices except for a last memory slice contain a respective
9 default location initialized to zero which serves as a padding value to said system bus of said
10 predetermined register width, when the respective last memory location of said memory slices is
11 accessed by said Micro-Engine.

1 8. The host-fabric adapter as claimed in claim 2, wherein, when a register width
2 requirement is 32 bits, and a system architecture requires 15 registers of 8 bits, 8 registers of 12
3 bits, and 17 registers of 32 bits for a total of 40 registers, said context memory having a
4 bandwidth optimized, vertically sliced memory architecture is partitioned into three memory
5 slices, including Memory A of 40x8 registers arranged to supply first 8 bits of 32-bit data, via a
6 system bus of 32 bits, Memory B of 25x4 registers arranged to supply next 4 bits of 32-bit data,
7 via said system bus of 32 bits, and Memory Z of 17x20 registers arranged to supply last 20 bits of
8 32-bit data, via said system bus of 32 bits, wherein said Memory B and Memory Z each contains

1 an additional default, last memory location initialized to zero which serves as a padding value to
2 said system bus of 32 bits, when the respective default, last memory location of a respective
3 memory slice is accessed by said Micro-Engine.

1 9. The host-fabric adapter as claimed in claim 2, wherein, when a register width
2 requirement is 32 bits and a system architecture requires 5 registers of 8 bits, 10 registers of 12
3 bits, 15 registers of 24 bits and 20 registers of 32 bits for a total of 50 registers, said context
4 memory having a bandwidth optimized, vertically sliced memory architecture is partitioned into
5 four memory slices, including Memory A of 50x8 registers arranged to supply first 8 bits of 32-
6 bit data, via a system bus of 32 bits, Memory B of 45x4 registers arranged to supply next 4 bits of
7 32-bit data, via said system bus of 32 bits, Memory C of 35x12 registers arranged to supply next
8 12 bits of 32-bit data, and Memory Z of 20x8 registers arranged to supply last 8 bits of 32-bit
9 data, via said system bus of 32-bits, wherein said Memory C, Memory B and Memory Z each
10 contains an additional default, last memory location initialized to zero which serves as a padding
11 value to said system bus of 32 bits, when the respective default, last memory location of a
12 respective memory slice is accessed by said Micro-Engine.

1 10. A host-fabric adapter installed at a host system for connecting to a switched fabric
2 of a data network, comprising:

1 at least one Micro-Engine (ME) arranged to establish connections and support data
2 transfers via said switched fabric;
3 a serial interface arranged to receive and transmit data packets from said switched fabric
4 for data transfers;
5 a host interface arranged to receive and transmit host data transfer requests, in the form of
6 descriptors, from said host system for data transfers;
7 a context memory having a bandwidth-optimized, area-minimal vertically sliced memory
8 architecture arranged to store context information needed for said Micro-Engine (ME) to process
9 host data transfer requests for data transfers; and
10 a doorbell manager arranged to update the context information needed for said Micro-
11 Engine (ME) to process host data transfer requests for data transfers.

1 11. The host-fabric adapter as claimed in claim 10, wherein said context memory
2 contains a large quantities of context registers arranged to store context information needed for
3 said Micro-Engine (ME) to process said host data transfer requests for data transfers.

1 12. The host-fabric adapter as claimed in claim 10, wherein said context memory
2 having a bandwidth-optimized, area-minimal vertically sliced memory architecture is partitioned
3 vertically into multiple memory slices based on a register width requirement, each of which
4 supplies respective bits of data of a predetermined register width to said Micro-Engine (ME), via

1 a system bus of said predetermined register width, and a total number of registers of said multiple
2 memory slices corresponds to a designated number needed by network device requirements.

1 13. The host-fabric adapter as claimed in claim 10, wherein said context memory
2 having a bandwidth-optimized, area-minimal vertically sliced memory architecture is partitioned
3 vertically into multiple memory slices based on a register width requirement, each of said
4 memory slices contains registers corresponding to a total number of registers provided by data
5 network requirements, each of said memory slices has a register width selected to supply
6 respective bits of data to said Micro-Engine (ME), via a system bus of a predetermined register
7 width, and a register depth selected to correspond to the total number of registers provided, and
8 all of said memory slices except for a last memory slice contain a respective default location
9 initialized to zero which serves as a padding value to said system bus of said predetermined
10 register width, when the respective last memory location of said memory slices is accessed by
11 said Micro-Engine.

1 14. The host-fabric adapter as claimed in claim 10, wherein said Micro-Engine (ME),
2 said serial interface, said host interface, said context memory, and said doorbell manager are
3 implemented as part of an Application Specific Integrated Circuit (ASIC).

1 15. The host-fabric adapter as claimed in claim 10, wherein, when a register width
2 requirement is 32 bits, and a system architecture requires 15 registers of 8 bits, 8 registers of 12
3 bits, and 17 registers of 32 bits for a total of 40 registers, said context memory having a
4 bandwidth optimized, vertically sliced memory architecture is partitioned into three memory
5 slices, including Memory A of 40x8 registers arranged to supply first 8 bits of 32-bit data, via a
6 system bus of 32 bits, Memory B of 25x4 registers arranged to supply next 4 bits of 32-bit data,
7 via said system bus of 32 bits, and Memory Z of 17x20 registers arranged to supply last 20 bits of
8 32-bit data, via said system bus of 32 bits, wherein said Memory B and Memory Z each contains
9 an additional default, last memory location initialized to zero which serves as a padding value to
10 said system bus of 32 bits, when the respective default, last memory location of a respective
11 memory slice is accessed by said Micro-Engine.

1 16. The host-fabric adapter as claimed in claim 10, wherein, when a register width
2 requirement is 32 bits and a system architecture requires 5 registers of 8 bits, 10 registers of 12
3 bits, 15 registers of 24 bits and 20 registers of 32 bits for a total of 50 registers, said context
4 memory having a bandwidth optimized, vertically sliced memory architecture is partitioned into
5 four memory slices, including Memory A of 50x8 registers arranged to supply first 8 bits of 32-
6 bit data, via a system bus of 32 bits, Memory B of 45x4 registers arranged to supply next 4 bits of
7 32-bit data, via said system bus of 32 bits, Memory C of 35x12 registers arranged to supply next
8 12 bits of 32-bit data, and Memory Z of 20x8 registers arranged to supply last 8 bits of 32-bit

1 data, via said system bus of 32-bits, wherein said Memory B, Memory C and Memory Z each
2 contains an additional default, last memory location initialized to zero which serves as a padding
3 value to said system bus of 32 bits, when the respective default, last memory location of a
4 respective memory slice is accessed by said Micro-Engine.

1 17. A method of designing a context memory having a bandwidth-optimized, area-
2 minimal vertically sliced memory architecture, comprising:

3 determining a register width requirement and a system architecture requirement of
4 registers of different sizes designated for said context memory;

5 selecting a number of vertically arranged memory slices of registers of different sizes
6 based on the register width requirement and the system architecture requirement such that each
7 memory slice has a number of registers provided by said system architecture and is arranged to
8 supply respective bits of data, via a system bus of said register width requirement;

9 determining the depth of each of said memory slices based on the respective number of
10 registers provided by said system architecture; and

11 establishing a default location that is initialized to zero ("0") in all subsequent memory
12 slices which serves as a padding value when a memory location of a respective memory slice
13 exceeding a register width of said memory slice is accessed, via said system bus.

1 18. The method as claimed in claim 17, wherein said context memory is arranged to
2 store context information needed for one or more Micro-Engines (MEs) in a host-fabric adapter
3 to process host data transfer requests for data transfers.

1 19. The process as claimed in claim 17, wherein, when a register width requirement is
2 32 bits, and a system architecture requires 15 registers of 8 bits, 8 registers of 12 bits, and 17
3 registers of 32 bits for a total of 40 registers, said context memory having a bandwidth optimized,
4 vertically sliced memory architecture is partitioned into three memory slices, including Memory
5 A of 40x8 registers arranged to supply first 8 bits of 32-bit data, via a system bus of 32 bits,
6 Memory B of 25x4 registers arranged to supply next 4 bits of 32-bit data, via said system bus of
7 32 bits, and Memory Z of 17x20 registers arranged to supply last 20 bits of 32-bit data, via said
8 system bus of 32 bits, wherein said Memory B and Memory Z each contains an additional
9 default, last memory location initialized to zero which serves as a padding value to said system
10 bus of 32 bits, when the respective default, last memory location of a respective memory slice is
11 accessed by said Micro-Engine.

1 20. The process as claimed in claim 17, wherein, when a register width requirement is
2 32 bits and a system architecture requires 5 registers of 8 bits, 10 registers of 12 bits, 15 registers
3 of 24 bits and 20 registers of 32 bits for a total of 50 registers, said context memory having a
4 bandwidth optimized, vertically sliced memory architecture is partitioned into four memory

1 slices, including Memory A of 50x8 registers arranged to supply first 8 bits of 32-bit data, via a
2 system bus of 32 bits, Memory B of 45x4 registers arranged to supply next 4 bits of 32-bit data,
3 via said system bus of 32 bits, Memory C of 35x12 registers arranged to supply next 12 bits of
4 32-bit data, and Memory Z of 20x8 registers arranged to supply last 8 bits of 32-bit data, via said
5 system bus of 32-bits, wherein said Memory B, Memory C and Memory Z each contains an
6 additional default, last memory location initialized to zero which serves as a padding value to
7 said system bus of 32 bits, when the respective default, last memory location of a respective
8 memory slice is accessed by said Micro-Engine.